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| 10/784,918 | 02/24/2004 | Naoki Takada | 62807-166 | 1966 |

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| EXAMINER | |
|---|---|
| SHERMAN, STEPHEN G | |
| ART UNIT | PAPER NUMBER |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/784,918 | TAKADA ET AL. | |
| | Examiner | Art Unit | |
| | Stephen G. Sherman | 2629 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *21 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *5-8 and 11-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-8 and 11-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 21 November 2007 has been entered. Claims 5-8 and 11-13 are pending. Claims 1-3 have been cancelled.

### *Response to Arguments*

2. Applicant's arguments with respect to claims 5-8 and 11-13 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 13 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The claim states that the data driver supplies the tone signal corresponding to the display data corresponding to spaces where said second clock is not created, however, display data is not supplied according to the applicant's specification. Instead, blanking data is supplied during this point of time. The applicant has not disclosed of display data being supplied when the clock is not created and therefor cannot claim this feature.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 5-7 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimoto et al. (US 2003/0090449) in view of Kanauchi et al. (US 6,788,277).

***Regarding claim 11***, Arimoto et al. disclose a display device, comprising:

a pixels array including a plurality of pixels arranged in a form of a matrix (Figure 9, LIQUID CRYSTAL PANEL 405);

a data driver for supplying a tone voltage corresponding to display data to the pixels (Figure 9, source driver 403);

a scan driver for selecting pixels of at least one row to which the tone voltage is to be supplied (Figure 9, gate driver 404); and

a control circuit for controlling the data driver and the scan driver (Figure 9, driving pulse generating section 902 and signal converting section 401), wherein:

the control circuit outputs a first clock signal and the display data to the data driver (Figure 9 shows that the signal converting section 401 outputs the display data and that driving pulse generating section 902 outputs a source driver control signal (first clock) to the source driver 403); and

the control circuit outputs to the scan driver a second clock signal, and outputs a scanning start signal generated a plurality of times during one frame period (Figure 9 shows that the driving pulse generating section 902 outputs a gate driver control signal

to the gate driver 404, where it is inherent that there will be a start pulse and also a clock signal, i.e. second clock, generated for scanning.).

Arimoto et al. fail to teach of the second clock signal not being created every n (n >2) signal creation thereof and that the control circuit outputs to the data driver blanking data other than the display data in place of the display data that corresponds to spaces where said second clock is not created.

Kanauchi et al. disclose of a display device containing a scanning clock signal not being created every n (n >2) signal creation thereof and that a control circuit outputs to a data driver blanking data other than display data in place of the display data that corresponds to spaces where said clock is not created (Figure 14 shows that every so many, i.e. n, creations of the scan clock signal the cock is not created denoted by the second labeled as stop, and that during this period of time black data is output.).

Therefore, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the teachings of not creating the clock as taught by Kanauchi et al. in the display device taught by Arimoto et al. in order to provided power savings when the blanking data is output.

***Regarding claim 5***, Arimoto et al. and Kanauchi et al. disclose the display device according to claim 11.

Arimoto et al. also disclose the display device further comprising:

a first memory for keeping the display data therein (Figure 5, line memory 502); and

a second memory for keeping the blanking data therein (Figure 5, non-image signal generating section 503), wherein:

the control circuit reads the display data from the first memory at timing synchronized with the first clock signal, outputs the display data to the data driver, reads from the second memory the blanking data corresponding to spaces where said second clock is not created, and outputs the blanking data to the data driver (Since the line memory 502 is output for normal display and the non-image signal generating section 503 is output from for blanking data, in combination of the references this would be output when the clock is not generated via the switch 504.).

***Regarding claim 6***, Arimoto et al. and Kanauchi et al. disclose the display device according to claim 11.

Arimoto et al. also disclose wherein a period of the first clock signal and a period of the second clock signal are synchronized with a scanning period for the scan driver to select pixels of at least one of the rows of pixels (Figure 10).

***Regarding claim 7***, Arimoto et al. and Kanauchi et al. disclose the display device according to claim 11.

Arimoto et al. also disclose wherein:

the scan driver sequentially selects one row of pixels in response to the second clock signal and selects the pixels twice for each row at a period of one frame in response to the scanning start signal (Figure 24);

the scan driver selects n rows of pixels corresponding to spaces where said second clock signal is not created (Figure 24 shows that the non-image signal is provided every 4 clocks, meaning in combination, the references teach of not creating the clock every 4 cycles, which is how many rows of pixels are selected as shown.);

the data driver supplies the tone voltage corresponding to the display data to the pixels of one row in response to the first clock signal (Figure 24 shows that the input image signal is provided which corresponds to display data for one row.); and

the data driver supplies the tone voltage corresponding to the blanking data to the pixels of n rows (Figure 24 shows that 4 rows receive the blanking data at a time.).

***Regarding claim 12***, Arimoto et al. and Kanauchi et al. disclose the display device according to claim 11.

Arimoto et al. also disclose where:

the scan driver selects the pixels of one row in response to the second clock signal and the scanning start signal during a period of time from a horizontal scanning period starting at timing at which the second clock signal is created immediately before the timing that corresponds to spaces where said second clock signal is not created (Figure 24 shows that the scan driver selects pixels of one row before blanking data is supplied, and based on the combination this is when the clock is not created.); and

the scan driver selects the pixels of n rows during one horizontal scanning period at which the second clock signal is created immediately before the timing at which the second clock signal is not created (Figure 24 shows that the non-image signal is

provided every 4 clocks, meaning in combination, the references teach of not creating the clock every 4 cycles, which is how many rows of pixels are selected as shown.).

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimoto et al. (US 2003/0090449) in view of Kanauchi et al. (US 6,788,277) and further in view of Park et al. (US 2002/0084959).

***Regarding claim 8***, Arimoto et al. and Kanauchi et al. disclose the display device according to claim 11.

Arimoto et al. and Kanauchi et al. fail to teach wherein the control circuit outputs to the scan driver a first scanning enable signal to invalidate selection of the pixels by the scan driver corresponding to spaces where said second clock signal is not created and a second scanning enable signal to validate selection of the pixels by the scan driver corresponding to spaces where said second clock signal is not created.

Park et al. discloses of a display device for supplying display data and blanking data, wherein there are multiple output enable signals where a first invalidates a selection and a second validates a selection (Figure 8 shows that when black data is output a scan pulse SP is output to the gate line GL32. When this occurs the enable signal GOE1 is high and "validates" the selection, while GOE2 is low and "invalidates" the section.).

Therefore, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the output enable signals taught by Park et al. in the

display device taught by the combination of Arimoto et al. and Kanauchi et al. in order to prevent crosstalk between adjacent pixel cells (Paragraph [0011] of Park).

***Conclusion***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Asada et al. (US 5,883,609) and Sekine (US 6,181,312) both disclose of not creating a clock signal when blanking data is supplied.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

17 December 2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER